HIGH EFFICIENCY SMALL SIZE 6W CLASS AB X-BAND POWER AMPLIFIER MODULE USING A NOVEL MBE GaAs FET

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ABSTRACT

A high efficiency 7.2 mm GaAs power FET using a novel doping profile grown by MBE was developed. This FET has achieved greater than 7 dB gain and 35.3 dBm power operating in class AB mode with a power-added-efficiency (P.A.E.) of 40% at 10.2 GHz. Extremely compact single and 2-stage balanced amplifier modules were developed achieving power, gain and P.A.E.'s of 37.7 dBm, 6.7 dB, and 34.8% for the single stage and 37.7 dBm, 15.1 dB, and 33.1% for the double stage amplifier modules at 1 and 2 dB gain compression points, respectively, across the 9.2-10.2 GHz band with good gain flatness and output return loss. The total 2-stage amplifier was realized on a carrier measuring only .700"x.280" by using high dielectric constant substrates for all the matching circuits. The values for the P.A.E. remained relatively constant with flange temperatures up to 75°C.

INTRODUCTION

The motivation for the development of this high power, high efficiency device was to meet the requirements for X-band airborne phased array systems. The applications include TWT replacement transmitters for passive phased array applications and in transmit/receive modules for active phased array radar applications. For both, the above applications power-added efficiency is of paramount importance since available prime power for airborne applications is very limited. Other requirements are high power density, high gain, small size, good output return loss and pulsed power operation. A pure class B mode of operation would have been ideal, since it eliminates bias synchronization problems with RF. Unfortunately, since g_m decreases near pinch-off, pure class B operation is not possible without a loss in gain. As a compromise between high efficiency and gain over a large dynamic range, class AB operation, where the quiescent drain current is about 20% I_{DSS}, was used in this application [1]. In order to satisfy these demands, a very high performance manufacturable FET was developed. This paper describes the development of the FET and the amplifier modules using these FETs. Performance characteristics of 25 devices are given to demonstrate the manufacturability of such a complicated device.

FET DEVELOPMENT

The key to high efficiency device performance is to optimize gain and breakdown voltage simultaneously. The material structure plays a very important part in this optimization. Generally, the gain increases with the doping level in the active channel layer. However, increased doping results in increased capacitance and lower breakdown voltages. The latter should be as large as possible for higher power and efficiency. One of the solutions is to tailor the doping profile in the channel; namely, a $N^+/N^-/N$ structure. The buried "N" layer increases the gain. The "N^-" layer in conjunction with a proper recess provides a higher breakdown voltage. The surface "N^+" layer provides for good ohmic contacts.

MBE Material Growth

The epitaxial layers for this study were grown by MBE in a Varian GEN II Modular system, on a 2" Cr-doped GaAs substrate. The epitaxial layers were grown at a nominal 600°C substrate temperature, using indium-free substrate holders. As_4 was used, with a beam flux monitor pressure ratio pAs_4/pGa of approximately 16. The growth rate was approximately 1 um/hour and the resulting surface morphology was excellent. A 1 um thick undoped buffer layer is grown first. The "N" layer is 850 Å thick doped in the range $2\text{-}3\times10^{17}$ cm^{-3}. The "N^-" layer is 2500 Å thick and is doped in the range $3\text{-}5\times10^{16}$ cm^{-3}. The surface contact "N^+" layer is 750 Å thick and doped to 3×10^{18} cm^{-3}.

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FET Design and Fabrication

The details of the device design and fabrication have been described elsewhere [2]. The gate fingers are 60x0.5 um and the channel spacing is 6.5 um. The total number of gate fingers is 120 and the pitch is 18.5 um. The device uses refractory gate metallization for increased reliability. Wraparound source grounding is used to reduce the source inductance.

FET Performance and Characterization

The FETs were mounted on a pre-matched copper carrier and evaluated at 10.2 GHz in a 50 ohm system with input and output coaxial tuners. Figure 1 shows the performance of the FETs from several wafers. The P_{out} is about 35 dBm with a P.A.E. greater than 37%, for a P_{in} of 28.5 dBm, with a best performance of 35.5 dBm, and 41%. This corresponds to .5W/mm power density. The FETs on pre-matched carriers were characterized under class AB conditions using empirical broadband load-source pull measurements, and simplified equivalent circuits for the input and output were extracted for matching purposes. The FET input circuit was a series RC (R=0.6 ohms, C=8 pF) and the output was a parallel RC (R=5.2 ohms, C=1.6 pF). The output conductance is lower than that predicted from simple load line concepts.

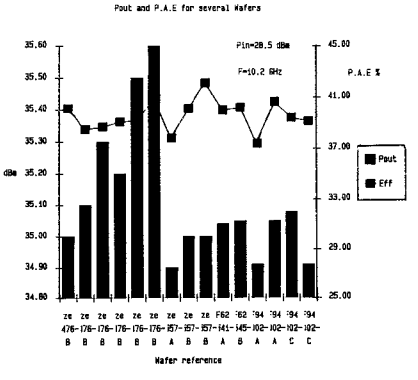

Figure 1. Power and Power-Added-Efficiency for the 7.2 mm Devices from 6 wafers

AMPLIFIER MODULE DESCRIPTION

The design target for the module was 5W output power, high efficiency for the case temperature range up to 75° C, and good output return loss. This dictated that the output stage consist of 2x7.2 mm FETs in a balanced configuration using 90° hybrid couplers. Class AB operating conditions were chosen in order to achieve higher efficiency. The optimal bias point for best power, gain, and efficiency was found to be Vdsq=9V and Idsq=20% I_{DSS}. Figures 2, 3, and 4 show the pictures of the three different amplifier versions 1, 2, and 3. All matching circuits were printed substrates with a E_r of 38 in order to achieve high circuit density. The version 2 amplifier consists of a 7.2 mm FET driving a balanced stage comprised of a pair of 7.2 mm FETs. The input and output circuit for each of the 7.2 mm FETs are exactly identical.

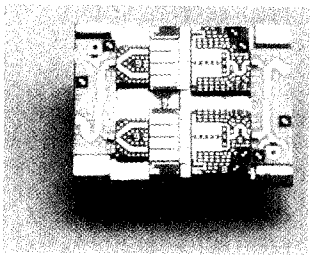

Figure 2. Picture of Version 1 Amplifier

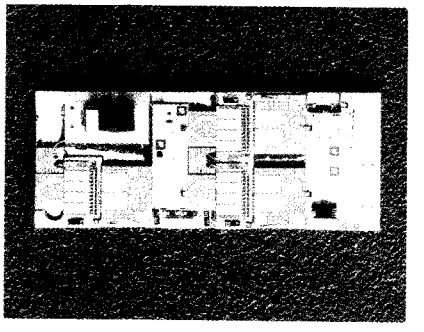

Figure 3. Picture of Version 2 Amplifier

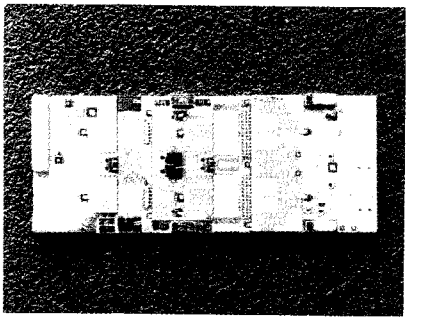

Figure 4. Picture of Version 3 Amplifier

The input circuit for each FET consists of gate bond wires series resonating the FET input capacitance. The resulting real input impedance is transformed to 50 ohms using distributed circuitry in order to minimize losses, circuit non-uniformity and for repeatability. The low impedance lines adjacent to the FET were realized on .003" (.076 mm) thick substate. The rest of the input circuit was on .013" (.33 mm) thick substrate.

The output circuit is also of a distributed nature and is realized on .013" (.33 mm) thick substrate. Part of the circuit is meandered in order to conserve space. The drain and gate bias were brought in on high impedance quarter wave lines to the output and input, respectively. The couplers were printed on .015" alumina. Silicon MOS capacitors were used for RF bypassing, DC blocking, and lowpass filtering for the bias rails in order to prevent spurious destructive oscillations. On-carrier thin film adjustable resistor bridges provide the correct gate bias from a common -5V rail. Although the driver FET is too big for optimal efficiency considerations, the overall performance was still impressive, as described later. This configuration was chosen for simplicity considerations in order to save design time.

The complete 2-stage module is mounted on a copper-tungsten carrier with dimensions of .700"x.280". A 1 uF tantalum capacitor is provided on the carrier for stability at frequencies in the MHz range. The carrier has no flange. Instead, pedestals protruding from the unused parts of the carrier are used to fixture the module for good thermal and electrical contact.

The version 3 amplifier consists of a pair of stages enclosed between Lange couplers for good input and output return loss. Each stage consists of a 3 mm device direct matched to a 7.2 mm device. The output circuit is the same as that of version 1. Part of the interstage match at the input of the larger device is on a .003" thick substrate and the rest is on .013" thick substrate. 50 pF MOS capacitors are used to provide the interstage DC blocking. No interstage tuning was necessary other than adjustment of the gate bond wires to the 7.2 mm FET. The input circuit for the 3 mm device is a scaled version of that for the 7.2 mm device in the version 2 amplifier. The gate bias voltage is adjusted separately for each pair of driver and output FETs, but each individual pair share the same voltage and, thus, have to be matched for DC. Both the version 2 and 3 amplifiers have no more than 5 nF drain bias filter capacitance in order to facilitate very fast pulse operation. For both versions, the tuning for optimum performance was very consistent and generally comprised of adjusting the input gate bond wires of the FETs and adding or removing pads at the output using gold wire bonds.

RF Performance

Version 1: Figure 5 shows the performance of the version 1 single stage balanced amplifier. The operating band is 9.2-10.2 GHz. The device delivered 37.7 dBm with 6.7 dB gain and 34.4% P.A.E. at 1 dB gain compression, at a T_{flange}=30°C, with a typical input and output return loss of 15 dB.

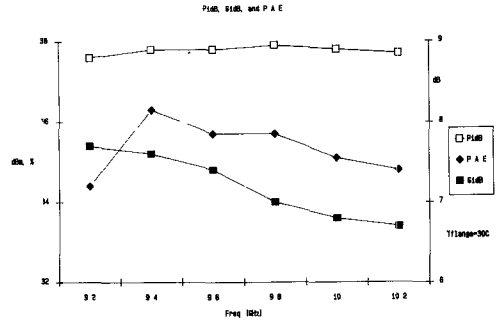

Figure 5. Power, Gain, and Power-Added-Efficiency of Version 1 Amplifier

Version 2: Figures 6 and 7 show the performance of a single unit. The 2-stage module delivered at least 37.7 dBm, 15.1 dB, and 32%, at a T_{flange}=30°C, and 37.2 dBm, 15.1 dB, and 32%, at a T_{flange}=75°C of power, gain, and P.A.E. at 2 dB gain compression, respectively, across the band. The performance of several amplifiers from FETs from 4 different wafers, at 30°C, is shown in figures 8, 9, and 10. As can be seen from the tight bunching, the performance is repeatable and consistent from devices within the wafer and from different wafers.

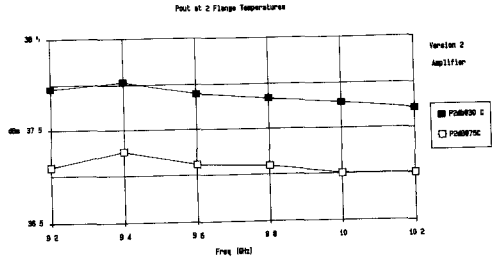

Figure 6. Power at 30°C and 75°C for Version 2 Amplifier

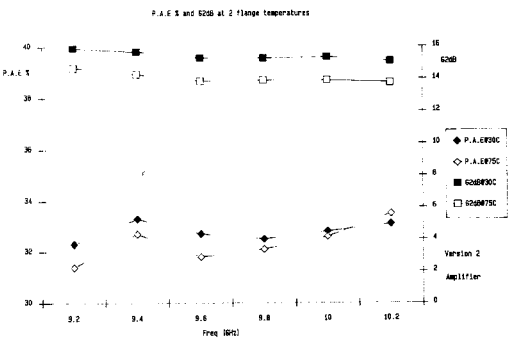

Figure 7. Power-Added-Efficiency and Gain at 30°C and 75°C for Version 2 Amplifier

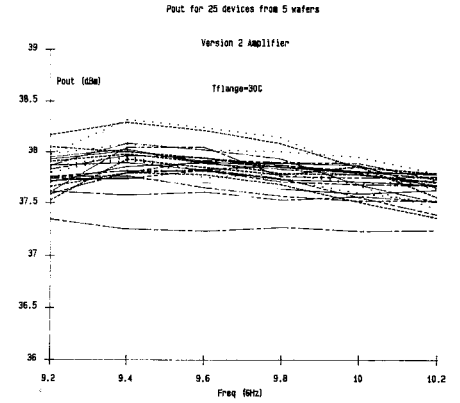

Figure 8. Power For Several Devices From 5 Wafers

Version 3: This device exhibited typical input return loss of 13 dB and output return loss of 15 dB. The power was similar to that of the version 1 amplifiers. Gain and P.A.E. were higher. This is due to lower losses in the interstage matching circuit, since the impedance locus does not have to go through 50 ohms as in the case of the version 2 amplifier, resulting in a lower Q matching circuit. At 10.2 GHz, a device exhibited 37.6 dBm, 15.5 dB, and 36% of power, gain, and P.A.E. at 2 dB gain compression.

SUMMARY

A high efficiency MBE FET using a novel doping profile has been developed. Three different versions of amplifiers have been built using these FETs and excellent RF performance has been obtained. To the best of the authors' knowledge, the efficiency and gain performance at 6W power levels presented above have not been reported in the literature to date [1]. This has been achieved, along with a good output return loss and excellent gain flatness of less than +/-0.5 dB. The module is extremely compact by using high E_r substrates and

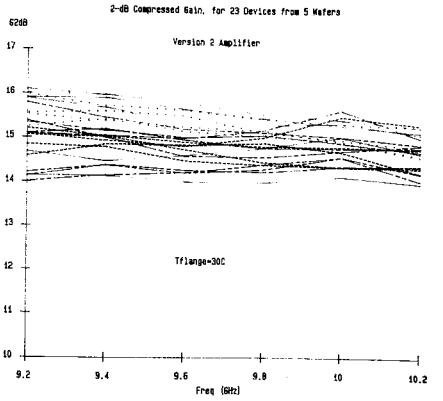

Figure 9. Gain For Several Devices From 5 Wafers

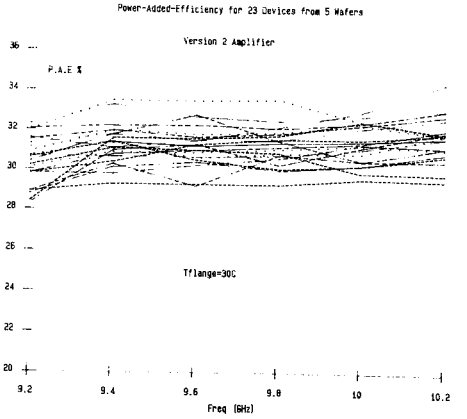

Figure 10. Power-Added-Efficiency For Several Devices from 5 Wafers

dense circuit packing. This module is specifically targeted for pulsed power applications in X-band phased array T/R modules where the factors such as high power, efficiency and small size are very important.

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REFERENCES

(1) J. R. Lane, R. G. Freitag, J. E. Degenford, and M. Cohn, "High Efficiency One, Two and Four Watt Class B FET Power Amplifiers," 1986 IEEE MTT-S Int. Microwave Symp. Dig., pp451-454.4

(2) M. Avasarala and D. S. Day, "2.5-watt and 5-watt Internally Matched GaAs FETs for 10.7-11.7 and 14-14.5 GHz Bands," 1986 IEEE MTT-S Int. Microwave Symp. Dig., pp455-458.